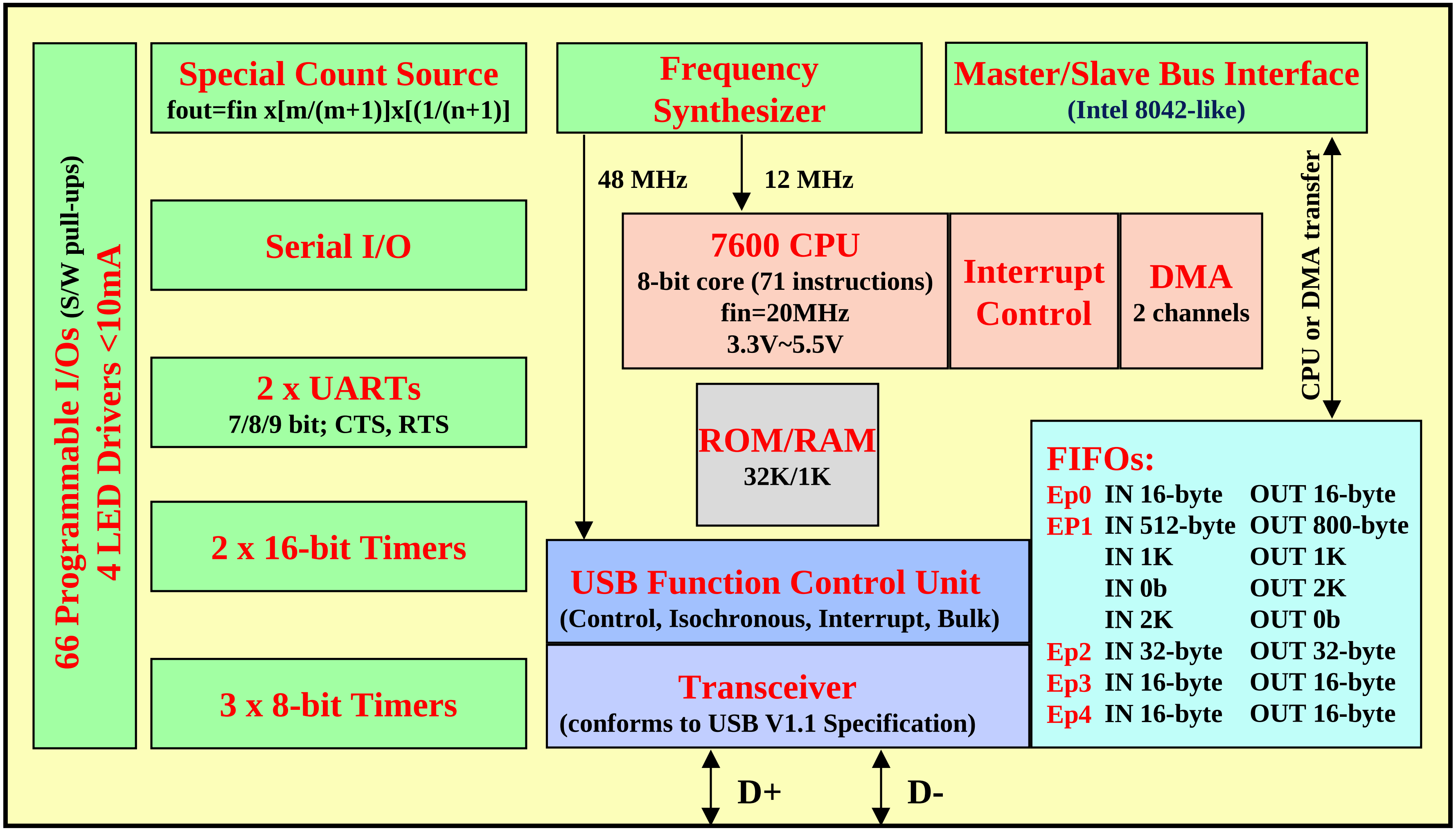
M37641M8
8-bit MCU
12Mbps USB

MITSUBISHI 8Bit Single-chip Microcomputer
740 Family / 764x

M37641 USB MCU Block Diagram



66 Programmable I/Os (S/W pull-ups)
4 LED Drivers <10mA

Special Count Source
fout=fin x[m/(m+1)]x[(1/(n+1)]

Serial I/O

2 x UARTs
7/8/9 bit; CTS, RTS

2 x 16-bit Timers

3 x 8-bit Timers

Frequency Synthesizer

48 MHz

12 MHz

Master/Slave Bus Interface
(Intel 8042-like)

CPU or DMA transfer

7600 CPU
8-bit core (71 instructions)
fin=20MHz
3.3V~5.5V

Interrupt Control

DMA
2 channels

ROM/RAM
32K/1K

USB Function Control Unit
(Control, Isochronous, Interrupt, Bulk)

Transceiver
(conforms to USB V1.1 Specification)

D+

D-

FIFOs:

Ep0	IN 16-byte	OUT 16-byte
EP1	IN 512-byte	OUT 800-byte
	IN 1K	OUT 1K
	IN 0b	OUT 2K
	IN 2K	OUT 0b
Ep2	IN 32-byte	OUT 32-byte
Ep3	IN 16-byte	OUT 16-byte
Ep4	IN 16-byte	OUT 16-byte

M37641 Highlights

- A high speed 5 endpoints USB function controller supports all USB transfer types: Isochronous, Bulk, Control and Interrupt.
- Isochronous Data Rate (via EP1):
  IN [(1000 Bytes out FIFO)/2] x 1000frames/msec x 8 = 4Mbps
  OUT [(1000 Bytes in FIFO)/2] x 1000frames/msec x 8 = 4Mbps
- Bulk Data Rate (via EP1): full bandwidth (64bytes/frame) supported.
- The built-in DC-to-DC converter eliminates the need of an external 3.3V power supply (converts from 4.15V~5.25V to 3.3V).
- The built-in analog transceiver (USB V1.1 Spec.) eliminates the need for an external device.
- Operates in both self-powered and bus-powered applications; also, remains powered during USB suspend mode using <200uA.

M37641 Highlights (con't)

- Two independent DMA channels provide an efficient means of transferring USB data between the USB FIFOs and other peripherals.

- The Intel 8042-compatible bus interface enables the M37641 to operate in a master/slave mode and to communicate with an external Host (or master) CPU at transfer rates up to ~3Mbytes; the Master is then free, while M37641 handles the local tasks.

- 8 Key-on Wake-up pins provide a way of returning from a STOP or WAIT mode.

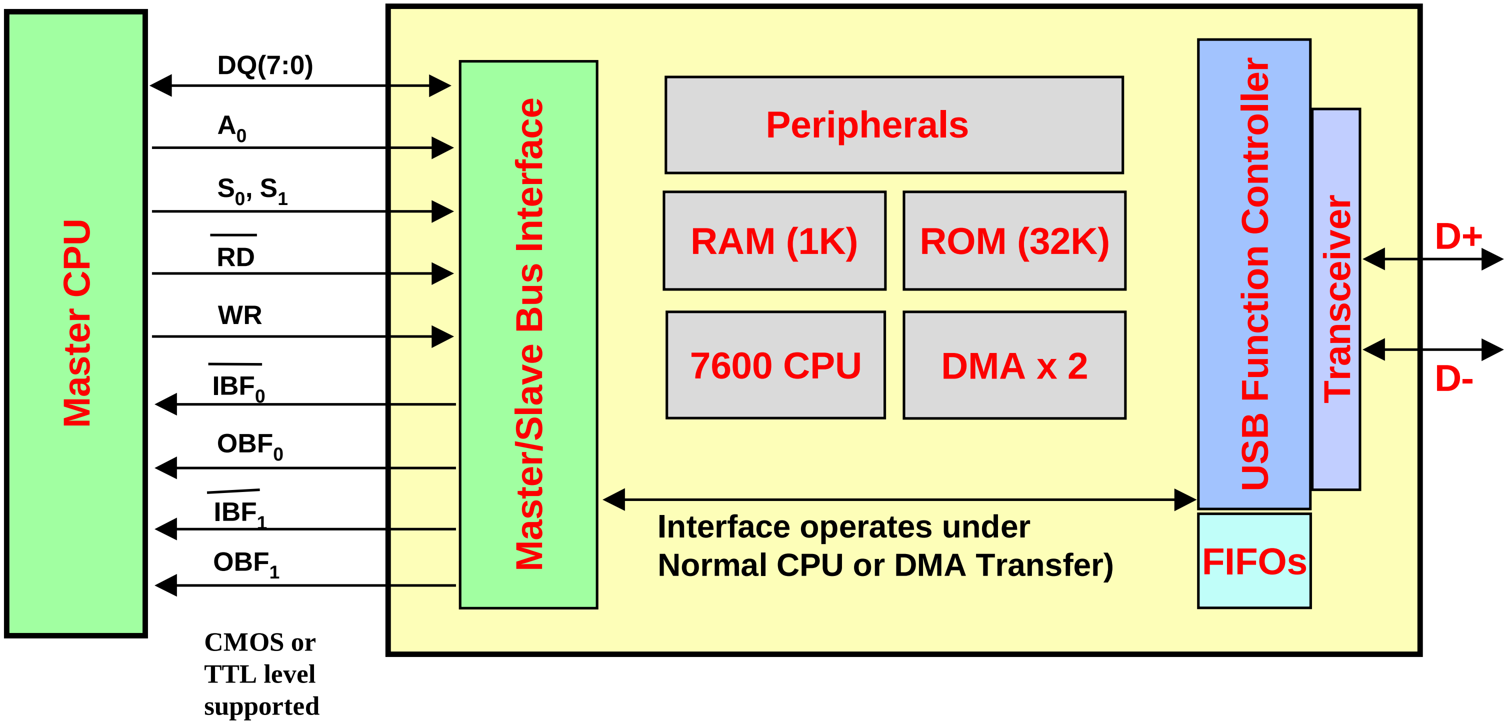
- Two different external clock inputs (Xin<24MHz and Xcin<5MHz) can be used for low-power operation mode or for keeping real time.

- An internal frequency multiplier provides the 48 MHz clock for the USB block and the CPU clock.

- A programmable special count source generator can be used to create various frequencies: fout=fin x[m/(m+1)]x[(1/(n+1)].

Master CPU I/F with M37641: 8042 compatible

- The MBI enables communication with a Master 16-bit or 32-bit CPU at transfer rates up to ~3Mbytes; the Master is then free, while M37640 handles the local tasks.
- Minimal external interface/decoding logic required (depending on the system)



Interface operates under Normal CPU or DMA Transfer)

CMOS or TTL level supported

Two-Channel DMAC Main Features

- Two independent channels closely coupled with the USB and the Master CPU Bus Interface for efficient data transfers.
- Two cycles of F required per byte transferred. F = 12MHz
- Single-byte (4Mbs) and burst transfer (6Mbs) modes
- Transfer requests from USB (9), Master CPU Bus Interface (4), external interrupts (4), UART1 (2), UART2 (2), SIO (1), TimerX (1), TimerY (1), Timer1 (1), and software triggers
- 16-bit source and destination address registers (for a 64 Kbyte adress space)
- 16-bit transfer count registers (for up to 64 Kbytes transferred before underflow)
- Source/Destination register automatic increment/decrement and no-change options
- Source/Destination/Transfer count register reload on write or after transfer count register underflow options.
- Fixed channel priority (Channel 0 > Channel 1)

Full-speed USB Function Controller V 1.1 (M37641)

- Complete Device Configuration
- Supports all Device Commands
- Support of All USB Transfer Types:
  - Isochronous, Bulk, Control, Interrupt
- Suspend/Resume Operation
- Self Powered Mode
- Error Handling capabilities
  - CRC Errors, Data Retries, Response Time-Out, ID Error

Full-speed USB Function Controller V 1.1 (M37641)

- FIFOs

Endpoint 0	IN 16-byte	OUT 16-byte	
Endpoint 1	IN 512-byte	OUT 800-byte	(mode 00)
	IN 1K	OUT 1K	(mode 01)
	IN 0b	OUT 2K	(mode 10)
	IN 2K	OUT 0b	(mode 11)
Endpoint 2	IN 32-byte	OUT 32-byte	
Endpoint 3	IN 16-byte	OUT 16-byte	
Endpoint 4	IN 16-byte	OUT 16-byte	

- Transfer Rates Examples for Endpoint 1

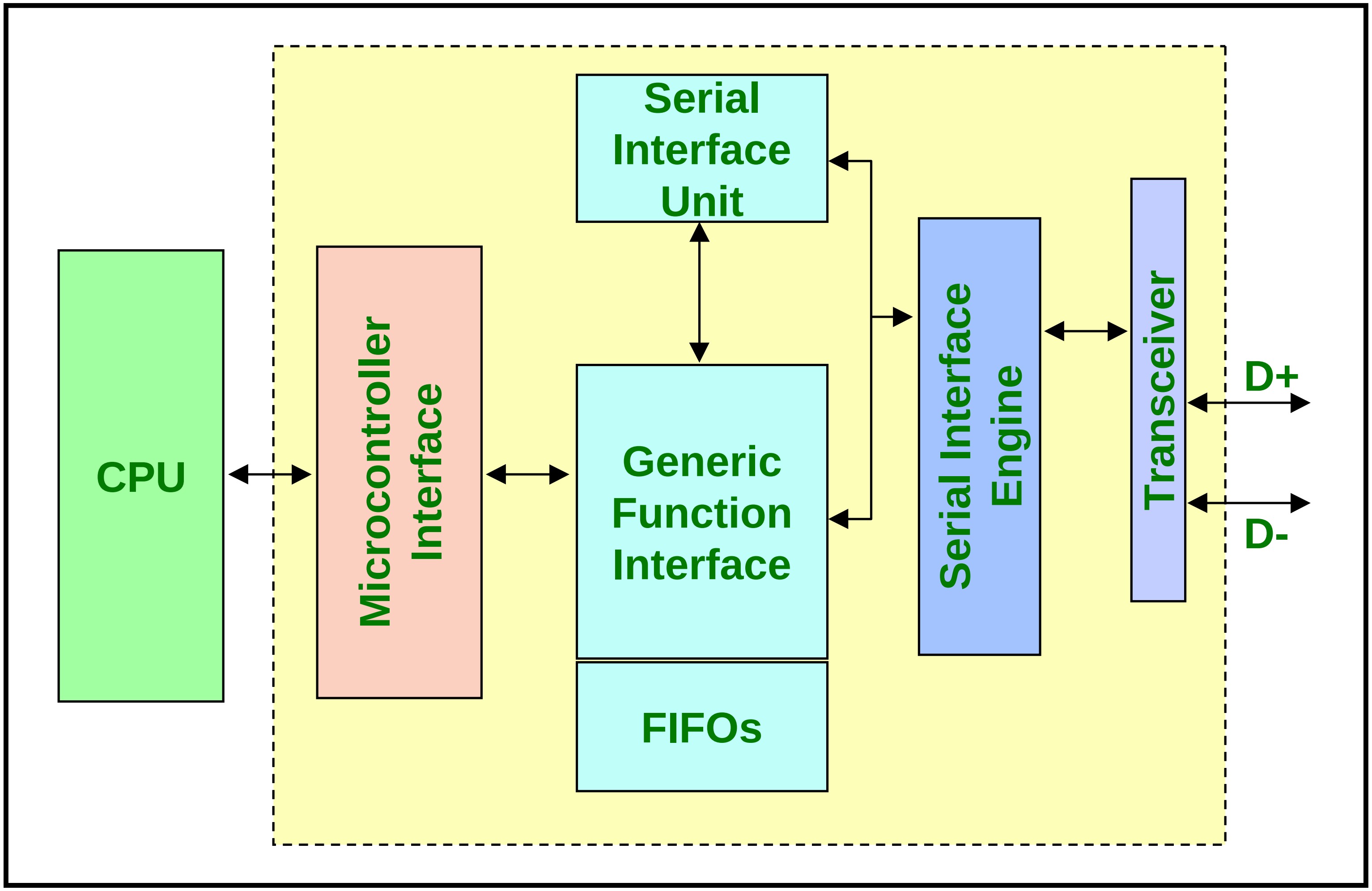
mode 00 IN [(512 Bytes out FIFO)/2] x 1000frames/msec x 8 = 2Mbps
OUT [(800 Bytes in FIFO)/2] x 1000frames/msec x 8 = 3.2Mbps

mode 01 IN [(1000 Bytes out FIFO)/2] x 1000frames/msec x 8 = 4Mbps
OUT [(1000 Bytes in FIFO)/2] x 1000frames/msec x 8 = 4Mbps

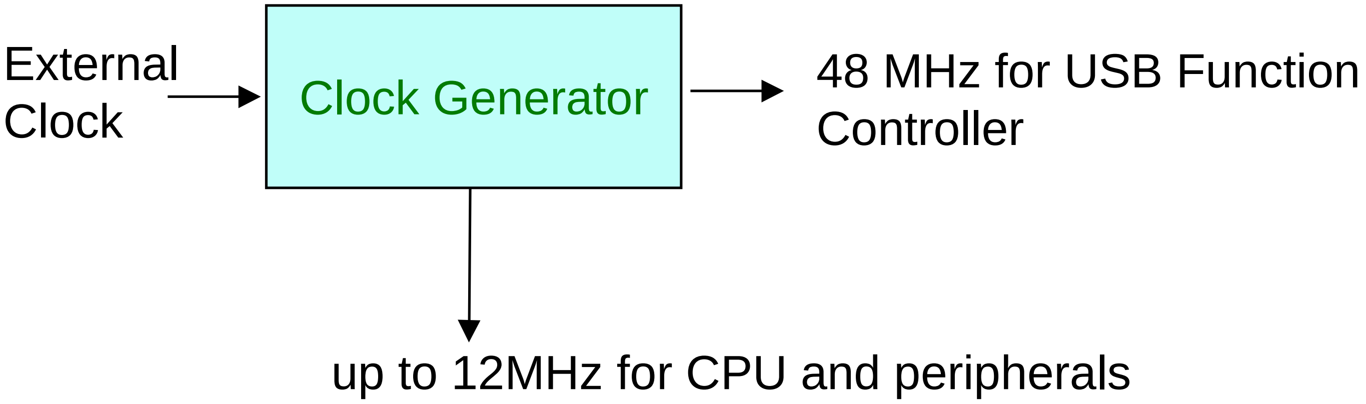
mode 10 IN [(0 Bytes out FIFO)/2] x 1000frames/msec x 8 = 0Mbps
OUT [(2000 Bytes in FIFO)/2] x 1000frames/msec x 8 = 8Mbps

mode 11 IN [(2000 Bytes out FIFO)/2] x 1000frames/msec x 8 = 8Mbps
OUT [(0 Bytes in FIFO)/2] x 1000frames/msec x 8 = 0Mbps

USB Function Controller Block Diagram (M37641)



Clock Generator (M37641)



External Clock

Clock Generator

48 MHz for USB Function Controller

up to 12MHz for CPU and peripherals

- 48MHz clock for USB eliminates expensive external clock oscillators
- On-chip clock generator minimizes EMI
- Generates MCU internal clock

M37641 Additional Features

- Slow Memory Wait
  When interfacing with external memory that is too slow to operate at the normal read/write speed of the MCU, a wait can be used to extend the read/write cycle.

- Hold Function
  The hold function is used when the MCU is put in a system where more than one device will need control of the external address and data buses.

- Expanded Data Memory Access
  The Expanded Data Memory Access (EDMA) mode feature allows the user to access greater than 64 Kbyte data, via a banking scheme.

Processor Modes

Single Chip Mode

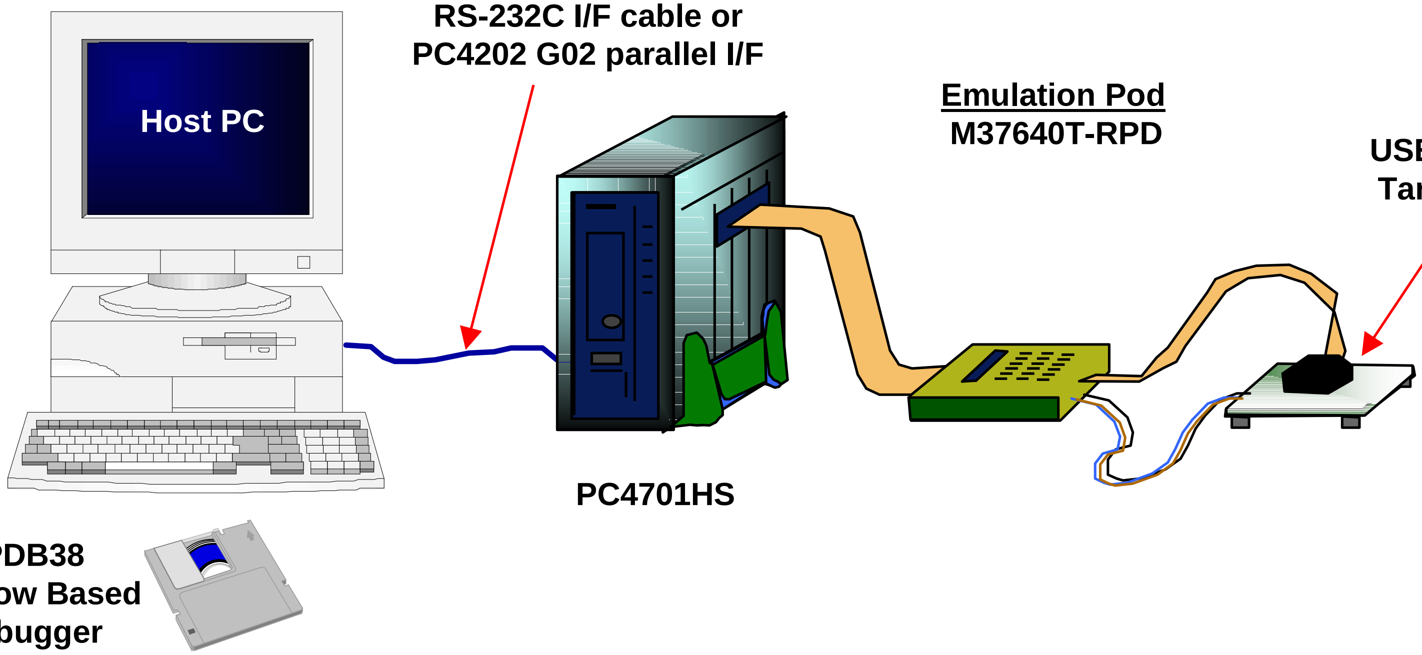
- All internal memory is accessible
- All dedicated pins behave as I/O ports

Memory Expansion Mode

- All internal memory is accessible
- External memory (up to 64K minus internal memory) can be accessed as well
- Four 8-bit ports become Address, Data and Control signals
- Slow memory wait and EDMA can be enabled

Enabling Quick System Development

- Peripheral Initialization S/W Routines
- Various Application Notes/Diagrams
- Erasable EPROM and OTP Devices
- Programming adapter
- In Circuit Emulator



Host PC

RS-232C I/F cable or
PC4202 G02 parallel I/F

Emulation Pod
M37640T-RPD

USER Defined
Target Board

PC4701HS

PDB38
Window Based
Debugger